Wafer level packaging of MEMS

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Abstract

Wafer level packaging plays important roles in practical applications of MEMS from the points of cost, size, yield and reliability. A silicon chip with MEMS on it can not be molded with plastics inherently on contrarily to a conventional integrated circuit. The MEMS have to be encapsulated in cavities by bonding a cover plate or by sacrificial etching and plugging the opening in wafer level. Since electrical interconnections have to be made from the cavity vertical interconnection through via or lateral interconnection on a chip are fabricated. Process compatibility is required especially for combining the MEMS and the integrated circuits. Various bonding techniques are used for the wafer level packaging. Vacuum packaging is required for some applications. Such detailed technical topics related to the wafer level packaging will be presented.